UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,676	12/04/2003	Sougo Ohta	10873.1331US01	8466

23552 7590 09/07/2005

MERCHANT & GOULD PC
P.O. BOX 2903
MINNEAPOLIS, MN 55402-0903

EXAMINER	
YAM, STEPHEN K	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/727,676	OHTA ET AL.	
	Examiner	Art Unit	
	Stephen Yam	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0204,0205*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 16 (Fig. 1, 10), 88 (Fig. 6). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 12 and 13 are objected to because of the following informalities:

In Claim 12, "1 x E^{17} cm^{-3}" is not a proper notation- the two proper notations are "1E17 cm^{-3}" or "1 x 10^{17} cm^{-3}".

In Claim 13, "5 x E^{18} cm^{-3}" is not a proper notation- the two proper notations are "5E18 cm^{-3}" or "5 x 10^{18} cm^{-3}".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al. US Pre-grant Publication No. 2004/0094784 in view of Applicant's admitted prior art (hereinafter AAPA) and Sasaki US Patent No. 4,471,525.

Regarding Claim 1, Rhodes et al. teach (see Fig. 1 and 6a) a solid-state imaging device (see Paragraph 0002), comprising a plurality of pixel cells (see Paragraph 0002 and 0007) that are laid out in matrix form on a semiconductor substrate (110, 120) (see Paragraph 0040), and a driving unit (sending signals to pixel transistors (40, 50, 60)) that is provided to drive the plurality of pixel cells, wherein each of the plurality of pixel cells includes a photodiode (120, 124, 126) (see Paragraph 0040) that converts incident light into a signal charge and stores the signal charge (see Paragraph 0041), at least one MOS transistor (50, 60) that is provided to read out the signal charge stored in the photodiode (see Paragraph 0006), and an element isolating portion (150), the element isolating portion being formed of a STI (Shallow Trench Isolation) (see Paragraph 0040) that is a grooved portion of the semiconductor substrate (see Fig. 6a), and in the semiconductor substrate, a STI leakage stopper (171, 173) (see Paragraph 0011-0015) in which an impurity of a conductive type (p-type) (see Paragraph 0047-0048) opposite to a conductive type (n-type) (see Paragraph 0007) of source/drain regions in the at least one MOS

transistor is introduced is formed to enclose a bottom face of the element isolating portion forming the grooved portion (see Fig. 6a). Rhodes also teaches using the element isolating portion at various locations to isolate other structures (see Paragraph 0038). Rhodes does not teach the element isolating portion formed so that the photodiode and each of the at least one MOS transistor are *isolated from each other*, or the STI leakage stopper enclosing *side walls* of the element isolating portion. Applicant's admitted prior art teaches (see Fig. 12-13) a solid-state imaging device with an element isolating portion (92) formed so that the photodiode and each of the at least one MOS transistor are isolated from each other (see Page 3, lines 4-7). Rhodes et al. and Applicant's admitted prior art do not teach the STI leakage stopper enclosing *side walls* of the element isolating portion. Sasaki teaches (see Fig. 8e) a semiconductor structure with an element isolating portion (47) (see Fig. 4c) being formed of a STI (Shallow Trench Isolation) (see Col. 15, lines 60-68) that is a grooved portion of the semiconductor substrate (111), with an STI leakage stopper (119) enclosing side walls and a bottom face of the element isolating portion forming the grooved portion (see Fig. 8e). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the element isolating portion formed so that the photodiode and each of the at least one MOS transistor are isolated form each other, as taught by Applicant's admitted prior art, and to provide the STI leakage stopper enclosing side walls of the element isolating portion, as taught by Sasaki, to isolate the various semiconductor elements to prevent electrical interference between the different elements, and to further isolate and capture the leakage current from the element isolating portion to minimize noise in the imaging device.

Regarding Claim 2, Tseng teaches the element isolating portion is formed so as to isolate the photodiode from another photodiode contained in a pixel cell adjacent to one of the plurality of pixel cells containing the photodiode (see Paragraph 0010, 0014, 0038).

Regarding Claims 4 and 5, Tseng teaches the STI leakage stopper having a thickness of not less than 0.01μm (100 Angstroms) or 0.02μm (200 Angstroms) (see Paragraph 0016).

Regarding Claim 11, Sasaki teaches the STI leakage stopper has a thickness that is larger at the bottom face of the element isolating portion than at the side walls of the element isolating portion (see Fig. 8e).

Regarding Claims 12 and 13, Tseng teaches the impurity introduced in the STI leakage stopper has a peak concentration of not less than $1x10^{17}$ cm^{-3} and as $5x10^{18}$ cm^{-3} (see Paragraph 0047, 0049).

Regarding Claim 3, Tseng in view of AAPA and Sasaki teach the device in Claim 1, according to the appropriate paragraph above. Tseng also teaches the at least one MOS transistor as a plurality of MOS transistors (see Paragraph 0006). Tseng also teaches the element isolating portion for isolating other structures (see Paragraph 0038, 0062). Tseng does not teach the element isolating portion formed so that one of the plurality of MOS transistors is isolated from another one of the plurality of MOS transistors. It is well known in the art to provide isolation between the different elements in a semiconductor device, to reduce cross-talk interference between elements. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the element isolating portion formed so that one of the plurality of MOS transistors is isolated from another one of the plurality of MOS transistors, in the device

of Tseng in view of AAPA and Sasaki, to improve isolation between the different elements of the pixel for reduced noise and greater sensitivity.

Regarding Claim 6, Tseng in view of AAPA and Sasaki teach the device in Claim 1, according to the appropriate paragraph above. Tseng does not teach the driving unit including a vertical driving circuit that drives the plurality of pixel cells along a row direction and a horizontal driving circuit that drives the plurality of pixel cells along a column direction. Applicant's admitted prior art teaches (see Fig. 10) an imaging device with a driving unit (12, 13) including a vertical driving circuit (12) that drives the plurality of pixel cells along a row direction and a horizontal driving circuit (13) that drives the plurality of pixel cells along a column direction. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a vertical driving circuit and horizontal driving circuit as taught by APPA in the device of Tseng in view of APPA and Sasaki, to provide addressing and readout for the pixels to effectively capture an image.

Regarding Claim 7, Tseng teaches the photodiode as an embedded photodiode in which a p layer (120), an n layer (126) and a p layer (124) are formed in this order starting from a surface side of the semiconductor substrate (see Fig. 6a), and the STI leakage stopper is formed so as to be linked to the p layer (120) of the photodiode (see Fig. 6a). Tseng does not teach the p layer (120) as a p+ layer. Applicant's admitted prior art teaches (see Fig. 16) the photodiode using a p+ layer (see Page 3, lines 23-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a p+ layer as taught by Applicant's admitted prior art in the device of Tseng in view of AAPA and Sasaki, to provide enhanced charge characteristics for the photodiode.

Regarding Claim 10, Tseng in view of AAPA and Sasaki teach the device in Claim 1, according to the appropriate paragraph above. Tseng does not teach a design rule for microfabrication of not more than 0.25μm is used for microfabrication of the plurality of pixel cells. It is well known in the art to use smaller microfabrication sizing, to reduce power consumption and increase transistor capacity on the semiconductor device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a design rule for <0.25μm microfabrication, in the device of Tseng in view of AAPA and Sasaki, to provide more transistor elements on the device and reduce power consumption.

5. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al. in view of AAPA and Sasaki, further in view of Yoneyama et al. US Patent No. 5,719,626.

Regarding Claims 8 and 9, Rhodes et al. in view of APP and Sasaki teach the device in Claim 1, according to the appropriate paragraph above. Tseng does not teach a MOS transistor constituting the driving unit as an NMOS transistor wherein the NMOS transistor constituting the driving unit form an NMOS dynamic logic circuit. Yoneyama et al. teach (see Fig. 1-3) an imaging device with a driving unit (see Col. 6, lines 18-24), wherein a MOS transistor constituting the driving unit as an NMOS transistor (see Col. 6, lines 25-29) wherein the NMOS transistor constituting the driving unit form an NMOS dynamic logic circuit (see Col. 6, lines 25-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a MOS transistor constituting the driving unit as an NMOS transistor wherein the NMOS transistor constituting the driving unit form an NMOS dynamic logic circuit, as

taught by Yoneyama et al., in the device of Rhodes et al. in view of AAPA and Sasaki, to provide a quick readout and reset/preset, as taught by Yoneyama et al. (see Col. 7, lines 58-62).

Allowable Subject Matter

6. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 14, the method of manufacturing a device as claimed (containing the limitations of the device of parent Claim 1), specifically in combination with forming a groove so that each of the at least one MOS transistor are isolated from each other, implanting ions into the groove so that the STI leakage stopper is formed to enclose *side walls* of the groove, forming the photodiode on the semiconductor substrate *after* the step of forming the element isolating portion, and forming the at least one MOS transistor such that each of the at least one MOS transistor is isolated from the photodiode by the element isolating portion, is not disclosed or made obvious by the prior art of record.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nozaki et al. US Patent No. 6,642,087 teaches an imaging device having an STI structure.

Tseng US Patent No. 5,801,082, teaches a STI structure with an STI leakage stopper enclosing side walls and a bottom face of the STI structure.

Morita US Patent No. 5,291,049, teaches a trench having a leakage stopper enclosing the side walls and a bottom face of the trench.

Chen et al. US Patent No. 6,118,142, teaches an imaging sensor having an STI structure and an insulator enclosing the side walls and a bottom face of the STI structure.

Chien et al. US Patent No. 6,281,081, teaches an STI structure with an STI leakage stopper enclosing side walls and a bottom face of the STI structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (571)272-2449. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571)272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SY

SY

THANH X. LUU
PATENT EXAMINER